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☐ 1. Document ID: US 20020169945 A1

Using default format because multiple data bases are involved.

L8: Entry 1 of 4 File: PGPB Nov 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020169945
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020169945 A1

TITLE: Microprocessor

PUBLICATION-DATE: November 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Haraguchi, Yoshiyuki	Tokyo		JP	

US-CL-CURRENT: 712/205; 712/234, 712/241

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20020083312 A1

L8: Entry 2 of 4 File: PGPB Jun 27, 2002

PGPUB-DOCUMENT-NUMBER: 20020083312
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020083312 A1

TITLE: Branch Prediction apparatus and process for restoring replaced branch history for use in future branch predictions for an executing program

PUBLICATION-DATE: June 27, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Sinharoy, Balaram	Poughkeepsie	NY	US	

US-CL-CURRENT: 712/240

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 3. Document ID: US 6745320 B1

L8: Entry 3 of 4 File: USPT Jun 1, 2004

US-PAT-NO: 6745320
DOCUMENT-IDENTIFIER: US 6745320 B1

TITLE: Data processing apparatus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 4. Document ID: US 5333280 A

L8: Entry 4 of 4 File: USPT Jul 26, 1994

US-PAT-NO: 5333280
DOCUMENT-IDENTIFIER: US 5333280 A

TITLE: Parallel pipelined instruction processing system for very long instruction word

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
(7 AND 2).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	4
(L7 AND L2).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	4

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Search Results - Record(s) 1 through 10 of 10 returned.

☐ 1. Document ID: US 6745320 B1

Using default format because multiple data bases are involved.

L13: Entry 1 of 10 File: USPT Jun 1, 2004

US-PAT-NO: 6745320
DOCUMENT-IDENTIFIER: US 6745320 B1

TITLE: Data processing apparatus

DATE-ISSUED: June 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mitsuishi; Naoki	Kodaira			JP

US-CL-CURRENT: 712/225; 711/212, 711/214, 712/201, 712/202, 712/203, 712/209, 712/227, 712/245

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 2. Document ID: US 6738893 B1

L13: Entry 2 of 10 File: USPT May 18, 2004

US-PAT-NO: 6738893
DOCUMENT-IDENTIFIER: US 6738893 B1

TITLE: Method and apparatus for scheduling to reduce space and increase speed of microprocessor operations

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 3. Document ID: US 6615339 B1

L13: Entry 3 of 10 File: USPT Sep 2, 2003

US-PAT-NO: 6615339
DOCUMENT-IDENTIFIER: US 6615339 B1

TITLE: VLIW processor accepting branching to any instruction in an instruction word

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set to be executed consecutively

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 4. Document ID: US 6564316 B1

L13: Entry 4 of 10 File: USPT May 13, 2003

US-PAT-NO: 6564316
DOCUMENT-IDENTIFIER: US 6564316 B1

TITLE: Method and apparatus for reducing code size by executing no operation instructions that are not explicitly included in code using programmable delay slots

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6370638 B1

L13: Entry 5 of 10 File: USPT Apr 9, 2002

US-PAT-NO: 6370638
DOCUMENT-IDENTIFIER: US 6370638 B1

TITLE: Apparatus and method of computer program control in computer systems using pipeline processing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6324639 B1

L13: Entry 6 of 10 File: USPT Nov 27, 2001

US-PAT-NO: 6324639
DOCUMENT-IDENTIFIER: US 6324639 B1

TITLE: Instruction converting apparatus using parallel execution code

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6275929 B1

L13: Entry 7 of 10 File: USPT Aug 14, 2001

US-PAT-NO: 6275929
DOCUMENT-IDENTIFIER: US 6275929 B1

TITLE: Delay-slot control mechanism for microprocessors

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 8. Document ID: US 5958044 A

L13: Entry 8 of 10 File: USPT Sep 28, 1999

US-PAT-NO: 5958044
DOCUMENT-IDENTIFIER: US 5958044 A

TITLE: Multicycle NOP

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 9. Document ID: US 5581778 A

L13: Entry 9 of 10 File: USPT Dec 3, 1996

US-PAT-NO: 5581778
DOCUMENT-IDENTIFIER: US 5581778 A

TITLE: Advanced massively parallel computer using a field of the instruction to selectively enable the profiling counter to increase its value in response to the system clock

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 10. Document ID: US 5398321 A

L13: Entry 10 of 10 File: USPT Mar 14, 1995

US-PAT-NO: 5398321
DOCUMENT-IDENTIFIER: US 5398321 A

TITLE: Microcode generation for a scalable compound instruction set machine

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
(12 AND 1).PGPB,USPT.	10
(L12 AND L1).PGPB,USPT.	10

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Refine Search

Search Results -

Term	Documents
NOP	867
NOPS	124
(10 AND NOP).PGPB.	8
(L10 AND NOP).PGPB.	8

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L14 an

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DATE: Wednesday, June 09, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB; PLUR=YES; OP=OR		
L14	l10 and nop	8	L14
	DB=PGPB,USPT; PLUR=YES; OP=OR		
L13	L12 and l1	10	L13
L12	(712/245)[CCLS]	490	L12
L11	(712/245)![CCLS]	490	L11
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L10	L9 and l2	60	L10
L9	L1 and nop	181	L9
L8	L7 and l2	4	L8
L7	L6 and l1	16	L7

h e b b cg b e e ch

L6	(end or last or least) near8 branch$3 near5 (portion$1 or field$1)	9690	L6
L5	L4 and l2	57	L5
L4	(NOP or (("no" or iddle) near2 operation$1)) near15 (branch or conditional or instruction) near5 (field$1 or portion$1)	218	L4
DB=PGPB,USPT; PLUR=YES; OP=OR			
L3	L2 and l1	70	L3
L2	(712/221-300)![CCLS]	4658	L2
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L1	(NOP or (("no" or iddle) near2 operation$1)) near15 (branch or conditional or instruction) near5 (field$1 or portion$1 or format)	256	L1

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1 **Walk-time address adjustment for improving the accuracy of dynan branch prediction**
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Computers, IEEE Transactions on , Volume: 48 , Issue: 5 , May 1999
Pages:457 - 469

[Abstract] [PDF Full-Text (524 KB)] **IEEE JNL**

2 **A concurrent fault detection method for superscalar processors**
Pawlovsky, A.P.; Hanawa, M.;
Test Symposium, 1992. (ATS '92), Proceedings., First Asian (Cat. No.TH0458 0) , 26-27 Nov. 1992
Pages:139 - 144

[Abstract] [PDF Full-Text (536 KB)] **IEEE CNF**

3 **Compiling Esterel into sequential code**
Edwards, S.A.;
Hardware/Software Codesign, 1999. (CODES '99) Proceedings of the Seventh International Workshop on , 3-5 May 1999
Pages:147 - 151

[Abstract] [PDF Full-Text (368 KB)] **IEEE CNF**

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branch and nop Search

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JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Walk-time address adjustment for improving the accuracy of dynan branch prediction**
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[Abstract] [PDF Full-Text (524 KB)] **IEEE JNL**

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